REMARKS

Claims 3-7 and 9-23 were previously pending in this application. Claims 3, 4, 6, 11, 15, 17, 19-21 and 23 have been amended. New claims 24-29 have been added. As a result claims 3-7 and 9-29 are pending for examination with claims 11, 15 and 24 being independent claims. No new matter has been added. For example, see page 6, line 22 and element 36 in Figure 1 for support concerning a "graphics accelerator chip."

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 3-7 and 9-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,678,002 to Frink et al. (hereinafter "Frink") in view of U.S. Patent No. 6,853,385 to MacInnis et al. (hereinafter "MacInnis").

The Office Action indicates and the Applicants agree that Frink "fails to disclose a graphics chip having at least two video inputs for respectively receiving said at least two real-time uncompressed digital video streams, said graphics chip further having a 2D graphics engine and a 3D rendering engine respectively for proving [sic] 2D and 3D functions used for video editing of said at least two real-time uncompressed digital video streams, said graphics chip further comprising a video output for providing edited uncompressed digital video streams." (Office Action at pages 3-4.) The Office Action, however, states that MacInnis discloses the preceding. (Office Action at page 4.)

Applicants respectfully assert that Frink and MacInnis each fail to teach or suggest the "graphics accelerator chip" recited in claim 11 or the "method of editing a plurality of video streams with a graphics accelerator chip" recited in claim 15 as amended herein. In particular, neither Frink nor MacInnis teach or suggest "a graphics accelerator chip having at least two video inputs for respectively receiving said at least two real-time uncompressed digital video streams," as recited in claim 11 or "[a] method of editing a plurality of video streams with a graphics accelerator chip … comprising acts of: receiving a first real-time uncompressed digital video stream at a first input of the graphics accelerator chip; [and] receiving a second real-time uncompressed digital video stream at a second input of the graphics accelerator chip," as recited in claim 15.

MacInnis describes a graphics processing system that may include a graphics accelerator 64. (Col. 6, lines 8-13 and Fig. 2.) The graphics accelerator 64 may be completely contained in

an integrated circuit chip. (Col. 60, lines 15-17.) Further, the graphics accelerator 64 receives commands from a CPU 22 and receives graphics data from main memory 28 through a memory controller 54. (Col. 60, lines 26-28.) Figure 4 illustrates that the graphics display pipeline 80 of MacInnis is separate from the video display pipeline 82.

The Office Action states that MacInnis describes a system "for providing 2D and 3D function [sic] of the uncompressed digital video as disclosed in Column 60 lines 1-30." (Office Action at page 4.) Applicants respectfully assert that the immediately preceding statement is not true, at least with respect to the graphics accelerator 64, because the graphics display pipeline of MacInnis operates on graphics data not video data. That is, the graphics accelerator 64 does not process video. Thus, although the results of graphics functions provided by the graphics display pipeline 80 may be composited with an output of the video display pipeline 82 (e.g., using video compositor 108 of Fig. 4), the graphics accelerator taught by MacInnis does not receive any real-time uncompressed digital video. Accordingly, MacInnis fails to teach or suggest that a graphics accelerator chip includes any video inputs for receiving a real time uncompressed digital video stream. The mere mention of employing a graphics accelerator to perform real-time 3D and 2D effects on graphics and video surfaces says nothing about "a graphics accelerator chip having at least two video inputs for respectively receiving said at least two real-time uncompressed digital video streams," as recited in claim 11.

In contrast, claim 11 recites an apparatus comprising "a graphics accelerator chip having at least two video inputs for respectively receiving said at least two real-time uncompressed digital video streams." Similarly, claim 15 recites "[a] method of editing a plurality of video streams with a graphics accelerator chip … comprising acts of: receiving a first real-time uncompressed digital video stream at a first input of the graphics accelerator chip; [and] receiving a second real-time uncompressed digital video stream at a second input of the graphics accelerator chip." Also in contrast to MacInnis, the graphics accelerator chip recited in claim 11 includes "a video output for providing edited uncompressed digital video streams." Neither Frink nor MacInnis teach or suggest anything about a graphics accelerator chip "comprising a video output for providing edited uncompressed digital video streams," as recited in claim 11. Also claim 15 recites an act of "generating an edited uncompressed digital video stream at a video output of the graphics accelerator chip" which neither Frink nor MacInnis teach or suggest.

Claims 11 and 15 are patentable in view of Frink and MacInnis at least for the reasons described above. Each of claims 3-7, 9, 10, 12-14, and 16-23 depend either directly or indirectly from one of claims 11 and 15. Accordingly, reconsideration and withdrawal of the rejection of claims 3-7 and 9-23 under 35 U.S.C. §103(a) as being unpatentable over Frink in view of MacInnis is respectfully requested.

New Claims

New independent claim 24 recites "a video editing apparatus for performing video editing in real time, the apparatus comprising: a graphics accelerator chip having at least two video inputs for respectively receiving at least two real-time uncompressed digital video streams, said graphics accelerator chip further having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams, said graphics accelerator chip further comprising a video output for providing edited uncompressed digital video streams."

Because neither MacInnis nor Frink teach or suggest anything about "a graphics accelerator chip having at least two video inputs … further comprising a video output for providing edited uncompressed digital video streams" as described above with reference to claim 11, claim 24 is allowable. New dependent claims 25-29 directly or indirectly depend from claim 24 and are also allowable for the preceding reasons.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50/2762, Ref. No. M1073-700719.

Respectfully submitted,
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